AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 11, 12, 13 and 15 as shown below.

Please **ADD** claims 16-24 as shown below.

The following is a complete list of all claims in this application.

1-10. (Cancelled)

11. (Currently Amended) A liquid crystal display (LCD), comprising:

a first substrate;

a gate line formed on the first substrate;

a data line formed on the first substrate and intersecting the gate line;

~~a pixel region defined by the gate line and the data line;~~

a storage capacitor line formed on the first substrate and crossing the data line; ~~and comprising~~

a storage capacitance electrode extending from the storage capacitor line along the data line;

a pixel electrode formed on the first substrate and entirely covering a portion of the storage capacitance electrode;

a second substrate facing the first substrate; and

a common electrode formed on the second substrate and having a first opening pattern overlapping the portion of the storage electrode entirely covered by the pixel electrode.

12. (Currently Amended) The LCD of claim 11, wherein the storage capacitor electrode is formed at a left side ~~and~~ or a right side of the pixel electrode ~~region~~.

13. (Currently Amended) The LCD of claim 11, wherein the storage capacitor line comprises two lines ~~in~~ crossing the pixel electrode ~~region~~.

14. (Previously Presented) The LCD of claim 11, wherein the pixel electrode has a second opening pattern comprising:

a first portion dividing the pixel electrode into an upper region and a lower region; and

second portions formed at the upper region and the lower region and proceeding perpendicular to each other.

15. (Currently Amended) A liquid crystal display, comprising:

a first substrate;

a second substrate facing the first substrate;

a pixel region;

a storage capacitor line formed on the first substrate and having a main portion and a branch portion extended from the main portion along a side of the pixel region;

a pixel electrode provided corresponding to the pixel region, insulated from the storage capacitor line and entirely covering a portion of the branch portion; and

a common electrode formed on the second substrate and having an opening pattern overlapping the portion of the branch portion entirely covered by the pixel electrode.

16. (New) A liquid crystal display (LCD), comprising:

a first substrate;

a second substrate facing the first substrate;

a plurality of gate lines formed on the first substrate;

a plurality of data lines intersecting the gate lines;

a pixel region defined by the intersecting of the gate lines and the data lines;

a first storage electrode line formed on the first substrate and extended along a first side of the pixel region;

a pixel electrode provided corresponding to the pixel region and entirely covering a portion of the first storage electrode; and

a common electrode formed on the second substrate and having an opening pattern overlapping the portion of the first storage electrode line entirely covered by the pixel electrode.

17. (New) The LCD of claim 16, further comprising a first storage capacitance line formed on the first substrate

18. (New) The LCD of claim 17, wherein the first storage electrode line is connected to the first storage capacitance line.

19. (New) The LCD of claim 17, further comprising a second storage electrode line extending along a second side of the pixel region.

20. (New) The LCD of claim 19, wherein the second storage electrode line is connected to the first storage capacitance line.

21. (New) The LCD of claim 19 , wherein the first storage electrode line and the second storage electrode line extend along the data lines.

22. (New) The LCD of claim 19, further comprising a second storage capacitance line formed on the first substrate.

23. (New) The LCD of claim 22, wherein the first storage capacitance line and the second storage capacitance line extend substantially parallel to the gate lines.

24. (New) The LCD of claim 23, wherein the first storage electrode line and the second storage electrode line interconnect the first storage capacitance line and the second storage capacitance line.